LISTING OF THE CLAIMS (1-25)

Claim 1 (previously presented): A semiconductor device comprising:
a plurality of multi level flash memory cells, wherein said cells have one erased state and three programmed states; and
wherein said cells are programmable from a first programmed state directly to a second programmed state by writing two bits of information to the cell being programmed.

Claim 2 (original): The semiconductor device as described in Claim 1 further comprising a page buffer, wherein said page buffer is for combining existing cell storage conditions with new partial page information.

Claim 3 (canceled)

Claim 4 (original): The semiconductor device as described in Claim 2 further comprising logic to combine said existing cell storage conditions with said new partial page information.

Claim 5 (original): The semiconductor device as described in Claim 4 wherein said logic is operable to produce allowable partial page program transitions.

Claim 6 (previously presented): A method of programming a partial page in a multi level flash device comprising:
a) presenting new programming information to said device;
b) reading existing cell storage conditions from said device;
c) combining said existing cell storage conditions with programming information to produce new information; and
d) programming said new information into said device, without an interposing erase operation.

Claim 7 (cancelled)

Claim 8 (original): The method as described in Claim 6 wherein said reading is automatically performed internally to said device.

Claim 9 (original): The method as described in Claim 6 wherein said existing cell storage conditions are copied into a page buffer.

Claim 10 (cancelled)

Claim 11 (original): The method as described in Claim 6 further wherein said combining is automatically performed internally to said device.

Claim 12 (original): The method as described in Claim 6 wherein said combining is performed in memory external to said device.

Claim 13 (original): The method as described in Claim 6 further wherein said combining takes place in a page buffer.

Claim 14 (currently amended): A semiconductor device comprising:

a plurality of flash memory cells, wherein said cells have one erased state and three programmed states; and

wherein said cells are programmable from a first programmed state directly to a second programmed state without an interposing erase operation by writing two bits of information to the cell being programmed.

Claim 15 (original): The semiconductor device as described in Claim 14 further comprising a page buffer, wherein said page buffer is for combining existing cell storage conditions with new partial page information.

Claim 16 (original): The semiconductor device as described in Claim 14 further comprising logic to combine said existing cell storage conditions with said new partial page information.

Claim 17 (original): The semiconductor device as described in Claim 16 wherein said logic is operable to produce allowable partial page program transitions.

Claim 18 (currently amended): A semi conductor device comprising:

a bus;

a plurality of external ports for receiving programming information coupled to said bus;

a plurality of memory cells, for the non-volatile storing of two bits of information, wherein said memory cells have one erased state and three programmed states, and are coupled to said bus;

a page buffer, for combining new programming information with previously stored information to produce program verify

~~information, wherein said page buffer is composed of pre-charged registers coupled to said bus~~; and

a state machine for placing new said programming information into said page buffer coupled to said bus;

said state machine also for placing previously stored information into said page buffer;

said state machine also for programming said program verify information into said memory cells by writing two bits of information to the cell being programmed.

Claim 19 (previously presented): A computer system comprising:

a processor coupled to a bus;

a first multi level cell flash memory coupled to said bus; and

wherein said computer system contains instructions which when implemented perform a method of programming a partial page in said first multi level cell flash memory, said method comprising:

a) presenting new programming information to said first multi level cell flash memory;

b) reading existing cell storage conditions from said device;

c) combining said existing cell storage conditions with programming information to produce new information; and

d) programming said new information into said first multi level cell flash memory, without an interposing erase operation.

Claim 20 (canceled)

Claim 21 (previously presented): The method as described in Claim 19 wherein said reading is automatically performed internally to said first multi level cell flash memory.

Claim 22 (original): The method as described in Claim 19 wherein said existing cell storage conditions are copied into a page buffer.

Claim 23 (canceled)

Claim 24 (original): The method as described in Claim 19 further wherein said combining is automatically performed internally to said first multi level cell flash memory.

Claim 25 (original): The method as described in Claim 22 wherein said computer system further comprises a second memory connected

to said bus, and wherein said combining is performed in said second memory.